Journal of Cardiovascular Disease Research

ISSN:0975-3583,0976-2833 VOL14,ISSUE05,2023

A COMPARATIVE STUDY OF VARIOUS 32-BIT CARRY SELECT ADDERS IN TERMS OF DELAY AND AREA

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Abstract: Design selection plays a vital role in selecting the most suitable adder for a particular application based on the requirements of delay and area. Particularly, with the advent of domain specific architectures, customized arithmetic operations are prevalent. Tailoring these adders for the specific application can enhance the performance and the efficiency of the specific architecture. These adders are essential for algorithmic customization. This paper discusses various techniques of carry select adders, Brent Kung adders. The gate count of 32-bit adders is calculated manually and the delay has been analyzed using Xilinx Vivado.
Index terms: Brent Kung adder, performance, carry select adder, Verilog, area, delay.

Introduction

With the introduction of domain specific architectures, the selection of adders for a particular application is essential to reduce the sparse in terms of performance and efficiency. This analysis can allow us to make the selection in a wise manner.
Although, carry select adder is used in various general purpose computer architectures. It does not give us enough efficiency in terms of delay over area. The combination of various adders with the carry select adder can optimize the adder performance. The gate level implementation of every adder architecture was implemented using Verilog HDL. In this paper we will implement carry select adder, modified carry select adder, Brent Kung adder with uniform carry select, Brent Kung adder without uniform carry select, carry select adder without mux, modified carry select adder with carry look ahead adder, carry look ahead adder with carry select adder without mux, Brent Kung adder without carry select adder.

Literature survey

Although there are many researchers who have implemented various adders, from the past six decades, there are only a few papers which talk comparative performance analyses of various adders in terms of area and delay. There are several advancements in the carry select adder to improve the efficiency either in terms of area or with respect to delay.
The quantitative analysis of these adders was performed using Verilog HDL in Xilinx Vivado. An explanation of how they are implemented, and implementation results are provided in the later sections.
Implementation of various adders

Carry select adder:

The carry select adder was implemented using primitive gates. The carry select adder was implemented using SQRT approach. This SQRT approach is implemented because full adder delay should be equal to mux delay to get the optimum delay.

ISSN:0975-3583,0976-2833 VOL14,ISSUE05,2023

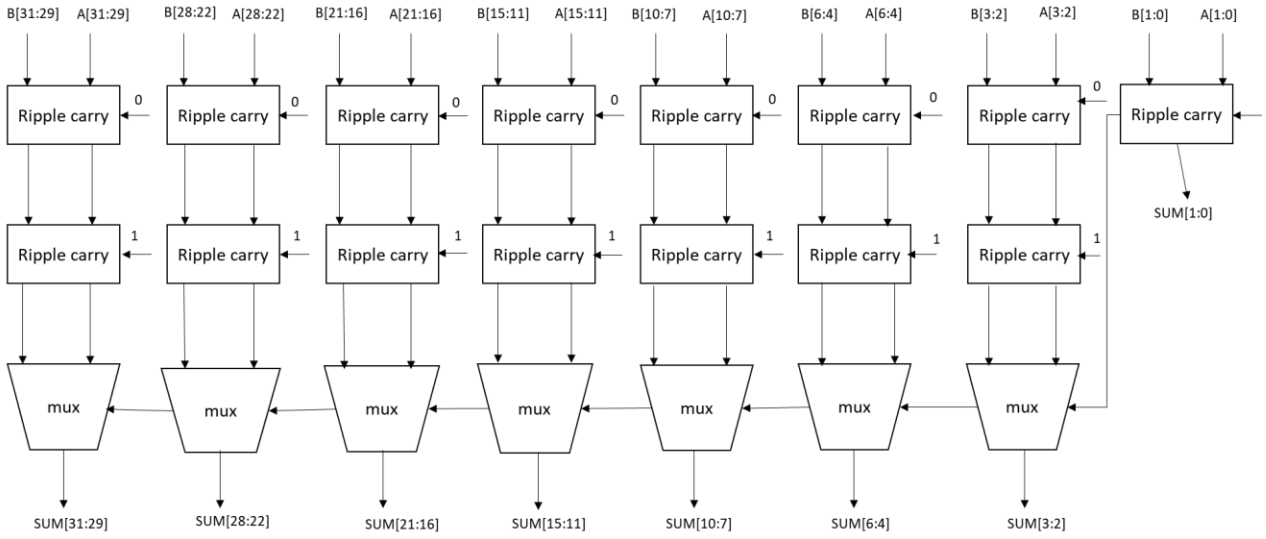

Fig1: 32-bit Carry select adder.

Carry Select adder does reduce the delay but occupies a huge area. So, it is always advisable to consider other options apart from carry select adder.

Modified carry select adder:

Modified carry select adder gives us the adder with reduced area with significant amount but there is little increment in the delay. In modified carry select adder ripple adder with input one is replaced with BEC (Binary to excess-1 converter). This is because BEC has reduced area when compared to ripple carry adder.

Carry select adder without mux:

The mux in the carry select adder is replaced with a combinational circuit which has the potential to reduce the area of the adder to a greater extent.

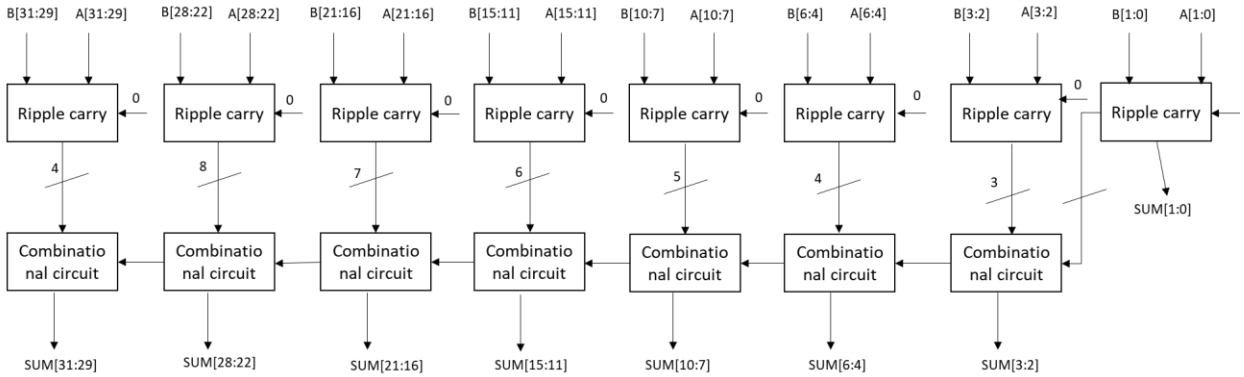

Fig2: 32-bit Carry select adder without mux.

The combinational circuit of the adder is implemented using the XOR gates and AND gates.

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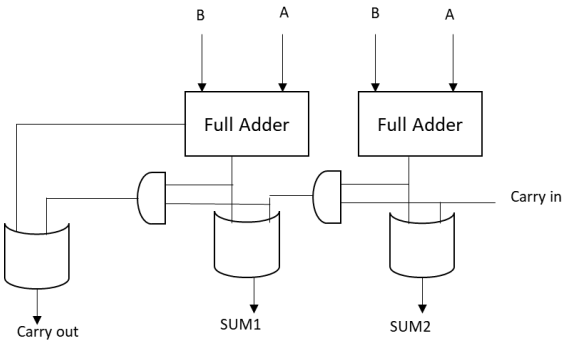

Fig3: Combinational circuit of the above carry select adder.

Modified carry select adder with carry look ahead adder:

The ripple carry adder in the modified carry select adder has been replaced by carry look ahead adder. In carry look ahead adder the carry can be generated independently without waiting for the previous carry. There are two major circuits in carry look ahead adder.

- Carry Generate – Gi = Xi and Yi
- Carry Propagate – Pi = Xi xor Yi
- Carry for the next bit – Ci+1 = Gi or (Pi and Ci)
- Sum – Si = Xi xor Yi xor Ci

This carry look adder's intricacy is one of its main flaws. Implementing a carry look-ahead adder with more than 4 bits is difficult. Therefore, in order to simplify the circuit, we developed a maximum modified carry look adder that is 4 bits wide in this carry select adder. The circuit that remains is identical to that of the modified carry select adder.

Modified carry select Brent Kung adder with uniform carry select:

The schematic design of normal Brent Kung adder was implemented with the following schematic circuit with the gray cells and black cells.

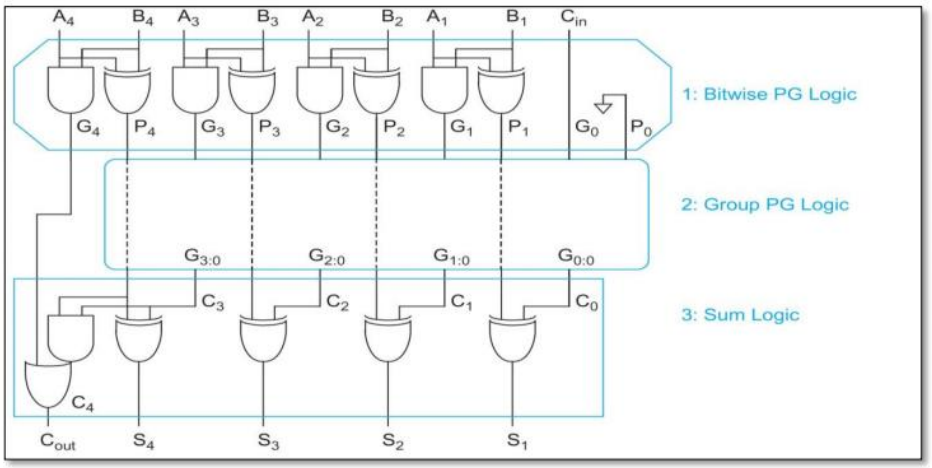

Fig 4: Brent Kung adder schematic

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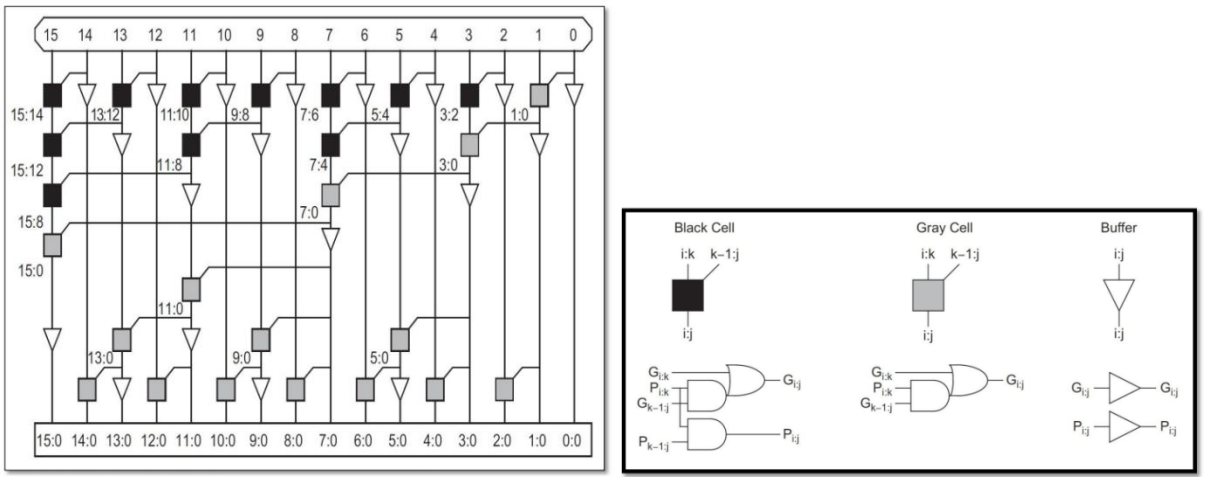

Fig 5: Group PG logic schematic with gray and black cells.

The above circuit shows 16- bit Brent Kung adder but we will use only 4-bit Brent Kung adder to reduce the complexity. We will use the carry select adder without the SQRT design but with uniform design. We will replace the ripple carry adder in modified carry select adder with Brent Kung adder.

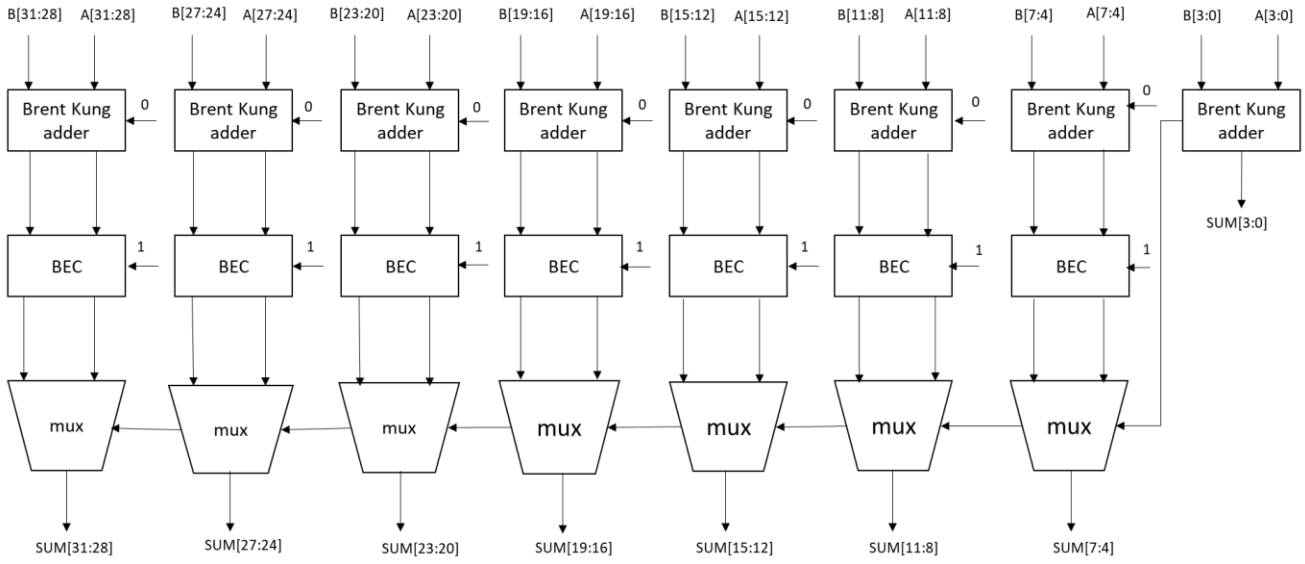

Fig 6: Modified carry select Brent Kung adder with uniform carry select.

Modified carry select Brent Kung adder with non – uniform carry select:

The modified carry select Brent Kung adder with non - uniform carry select contains the Brent Kung adder of varied bit size across the carry select adder. In non-uniform carry select we will use SQRT approach for the Brent-Kung adder with BEC circuit left intact.

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Results and discussion

The combination of various carry select adders have been implemented in Xilinx Vivado for analyzing the delay of each circuit. The above discussion demonstrates the implementation of these basic carry select circuits. We can implement it with various combinations and the possible combination implemented has been presented below.

The area utilization of each adder has been calculated by analyzing the number of gates utilized. This is calculated by considering AND, OR and NOT gates as 1 unit each.
XOR – 5
2 channel MUX – 4
Full Adder – 13
Below graphs depict the area and gate utilization of various carry select adders implemented.

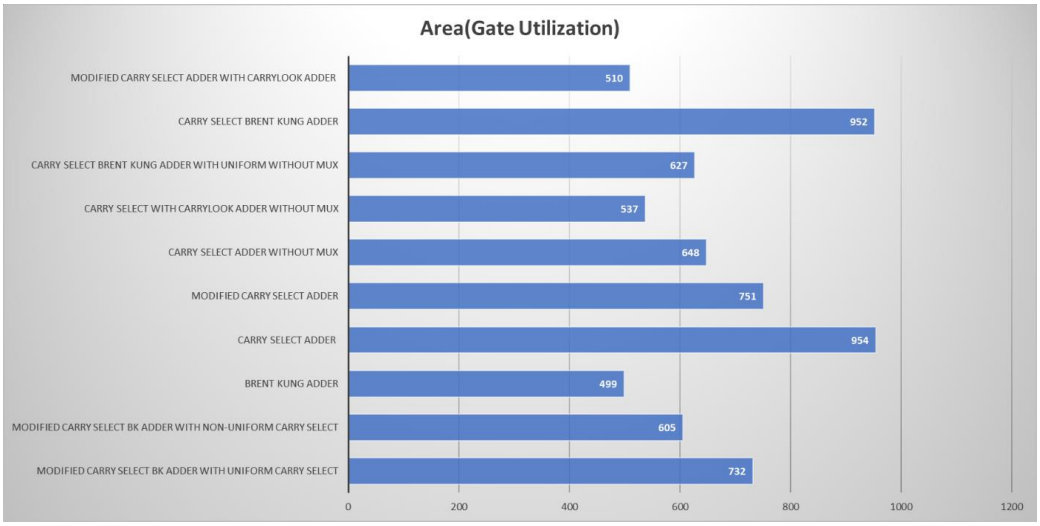

Fig 7: Gate utilization of various carry select adders.

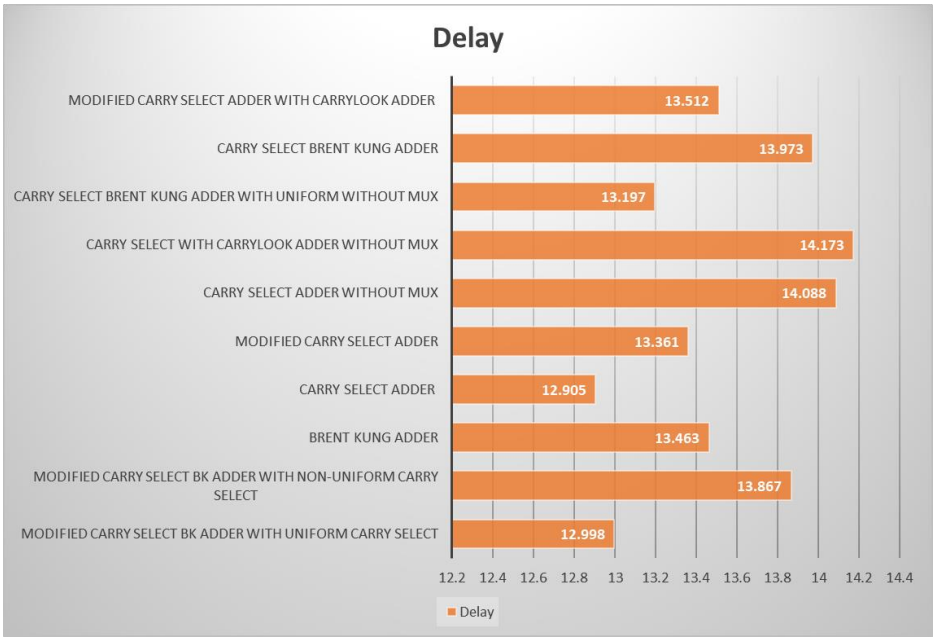

Fig 8: Delay of various carry select adders.

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Conclusion

The above analysis of various carry select adders will increase the selection of appropriate carry select adders according to the application. If we consider going with most optimized in terms of delay and area, Brent Kung adder with uniform carry select is better adder when compared to the remaining carry select adders. For the future domain specific architectures these carry select adders' selection is much required to improve the efficiency of the arithmetic computations.

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