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Streamlining Communication in Medical Device Networks with Aggregated CDMA Encoding/Decoding

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Abstract

Medical devices often rely on efficient communication protocols to transmit data within Network-On-Chip (NoC) architectures, ensuring fixed latency, guaranteed service, and reduced system complexity. One such protocol, Code Division Multiple Access (CDMA), originally designed for wireless communications, assigns each bit in a data word to a separate channel to prevent interference. However, in medical device interconnects, replicating CDMA channels can be unnecessary, addressing wireless interference concerns more efficiently. Furthermore, medical device interconnects typically utilize parallel buses rather than sequential channels for communication. Despite this difference, the medical device community has continued to employ the traditional wireless CDMA scheme, leading to duplicated encoding/decoding logic for data packets. This paper introduces a novel CDMA encoding/decoding scheme, termed Aggregated CDMA (ACDMA), tailored specifically for medical device interconnects. ACDMA consolidates the encoding of all packet bits into a single CDMA channel, thereby reducing the area and energy overheads associated with replicating encoding/decoding logic for multiple channels.

Keywords: Network-On-Chip, Code Division Multiple Access, Energy-Power Consumption.

I. INTRODUCTION

Modern Systems-on-chips (SoCs) are becoming massively parallel with many harmoniously interconnected Processing Elements (PEs). Interconnecting the PEs is commonly achieved through buses and Networks-on-Chips (NoCs) [1]. In NoCs, exchanged data is bundled into packets and traverse several network layers passing by the physical layer which defines how packets are transmitted between NoC units. The physical layer of a NoC is implemented by routers employing crossbar switches. Code Division Multiple Access (CDMA) is a medium sharing technique that leverages orthogonal codes to enable simultaneous packet routing. Unlike timeshared channels, CDMA leverages the code space to enable channel sharing. CDMA has been proposed as an on-chip interconnect technique for both bus and NoC interconnect architectures [2]. Many advantages of using CDMA for on chip interconnects include reduced power consumption, fixed communication latency, and reduced system complexity [3]. Utilizing CDMA in NoC interconnects is adopted from the wireless communications literature, where the data is spread by orthogonal codes at the transmitters, the spread data are added on the wireless channel, and the received sum is decoded at the receivers. Classical CDMA systems rely on the Walsh orthogonal code family to enable medium sharing. Many research groups have investigated several aspects of CDMA in NoCs, including our group which presented the Overloaded CDMA for on-chip Interconnects (OCI) [4] [5] [6]. A 14-node CDMA-based network has been developed in [7]. The network utilizes 7 Walsh codes

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and assignment of the Walsh codes to the network nodes is dynamic based on the request from each node. Two architectures have been introduced in [7]: a serial CDMA network where each data chip in the spreading code is sent in one clock cycle; and a parallel CDMA network where all data chips are sent in the same cycle. The serial and parallel CDMA-based networks have been compared to a conventional CDMA network, a meshbased NoC, and a Time Division Multiple Access (TDMA) bus. For the same network area, the throughput of the parallel CDMA network is higher than that of the mesh-based NoC and the TDMA bus due to the simultaneous medium access nature of CDMA. Standard-basis codes are proposed as a replacement to Walsh CDMA codes in [8]. Standard-basis codes resemble TDMA signaling because each code consists of only a single chip of one and the remaining chips are zeros. The TDMA codes' orthogonality enables them to replace the Walsh codes as spreading and despreading CDMA codes, which reduces the complexity of the channel adder and decoder as the sum of TDMA codes is limited to zero or one per clock cycle.

2. Literature Survey

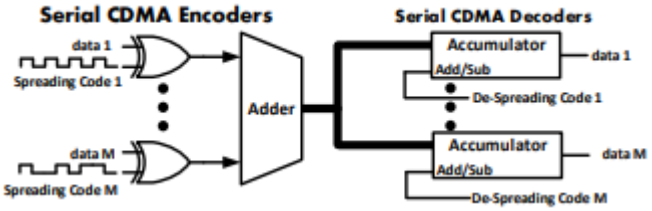

Figure 1. Conventional CDMA crossbar .

The conventional CDMA crossbar employed in the literature is depicted in Figure 1. The crossbar interconnects N transmit ports to N receive ports using N-chip length Walsh spreading codes. The binary data from each transmit port is encoded using an XOR encoder; the data bit is XORed with a unique N-chip spreading code assigned to the transmit-receive pair and transmitted in N clock cycles. Data spread from all encoders are added by the CDMA channel adder and sent to all receive port. The decoder at each receive port extracts the data from the channel sum by correlating the channel sum with the assigned spreading code. The correlation operation is implemented using an accumulator and a multiplexer since the despreading code chips are unipolar ("0" or "1"). In all of the CDMA interconnect related work, each data bit in a data word is encoded and transmitted in a separate CDMA channel and the encoding/decoding logic is replicated W times for data packets of width W which is a direct application of the wireless CDMA principles in NoC interconnects. However, wireless communication channels are sequential by nature due to the interference problem. Multiple access and MIMO techniques can enable concurrent data transmission on the same wireless channel at the expense of increasing the transmitter/receiver complexity. in on-chip interconnects, on the other hand, a single channel can be efficiently utilized to enable parallel data transmission as noise and interference effects can be efficiently mitigated [9]. In this work, we present a single channel, multi-bit CDMA crossbar namely Aggregated CDMA (ACDMA) NoC crossbar.

3. PROPOSED NOC CROSSBAR ARCHITECTURE

The ACDMA crossbar implements the psychical layer of the NoC by interconnecting N transmit (TX) ports to N receive ports where the data width of each port is W where W = log2 max(dj). The high-level

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architecture of the ACDMA crossbar illustrated in Figure 2(a) is composed of three main parts; encoders, channel adder, and decoders. The encoders spread data from each TX port using W XOR gates as shown in Figure 2(b). Instead of adding the spreading chips of the Walsh orthogonal code to the result in the encoder block as suggested by (2), this operation is postponed to the channel adder block in order to merge the channel adder with the spreading code adders. The output of each encoder is, therefore, limited to W-bit width. The encoder outputs are then added together to form the sum Si of (3). To minimize the critical path of the channel adder, the addition is done using a tree adder architecture as depicted by Figure 2(c) where the leafs of the tree are the encoders of each TX port, and the root of the tree is the channel sum output. Because there are N leafs, the height of the tree is log2(N). The width of the output wires from each adder in the tree is equal to the width of the input wires plus one to prevent overflows. Since the input to the firs level of adders is (W +1)- bit wide and the height of the adder tree is log2(N), then the width of the output wires at the root adder is W +1+log2(N). Pipeline registers are inserted after each stage in the tree to minimize the critical path of the channel. The sum Si is then sent to all the N decoders, a decoder per RX port.

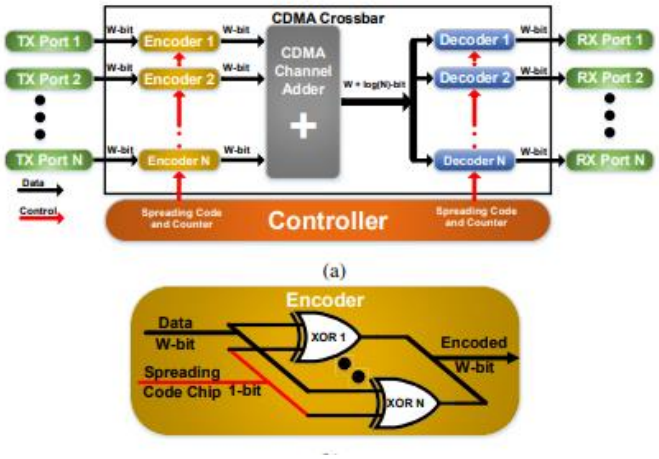

Figure 2. (a) ACDMA crossbar high-level architecture

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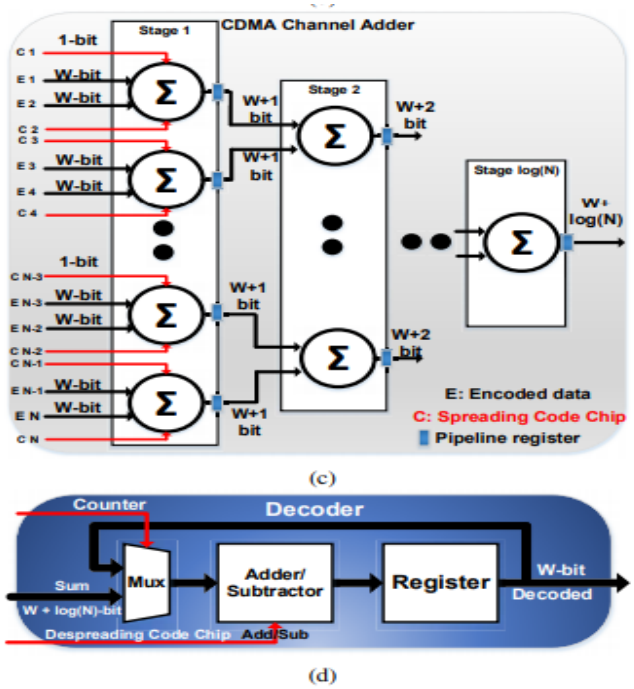

Figure 2. (c) ACDMA channel adder, (d)ACDMA decoder

The decoders implement the cross-correlation of (4) in a cost efficient manner; the decoder consists of only an adder/subtracter and a register configured as an up/down accumulator as shown in Figure 2(d). Since the despreading code Ck consists of ±1 chips, cross correlation is reduced to simple addition and subtraction operations of consequent sums Si . Therefore, the decoder is implemented as an up/down accumulator; the adder/subtracter adds or subtracts the sum Si from the result saved in the registers according to the value of despreading chip Ci k. In particular, when the despreading chip is '1', the adder adds Si to the contents of the register but subtracts Si from the contents of the register when the despreading chip is '-1'. At the end of the decoding cycle, the accumulator register holds N dk according to (5), and because N = 2n and n is an integer, data dk is decoded by shifting the accumulator content by log2(N) bits.

The number of two input XOR gates is the same for both circuits. The improvement of the ACDMA crossbar over the conventional CDMA crossbar is evident in the number of channel adder wires; in the conventional CDMA crossbar, the number of the adder wires for the single-bit channel is increased by one in each stage due to the additional carry bit. Therefore, the number of adder wires in stage i is equal to 1+log2(N)−i. For a W-bit word, the number of adder wires is increased to W+W(log2(N)−i), and since there are 2i adders at each stage, then the total number of wires is equal to log2N−1 i=0 2i (W +W(log2N −i)). In the ACDMA crossbar, conversely, the number of adder wires for a W-bit word is W +log2(N)−i, which makes the total number of wires equals to log2N−1 i=0 2i (W +log2N −i) which is a factor of W less than that of the conventional CDMA crossbar. The reduced number of carry bits of the ACDMA crossbar is the prime reason for its superiority. The number of wires for the decoder accumulator and the number of flip-flops in the decoder registers is proportional to the number of channel wires—the last

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stage of the adder. This follows that the complexity of the ACDMA crossbar is in an order of W less than that of the conventional CDMA crossbar.

3. Simulation Results

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	20	14752	0%
Number of Slice Flip Flops	19	29504	0%
Number of 4 input LUTs	31	29504	0%
Number of bonded IOBs	16	250	6%
Number of GCLKs	1	24	4%

Fig 3 Design summary

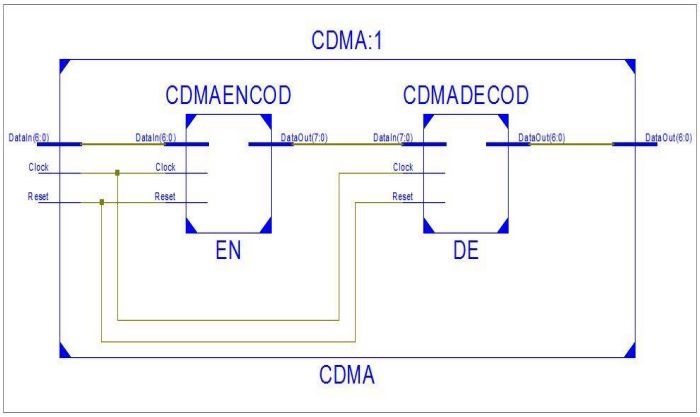

Fig 4. RTL Schematic

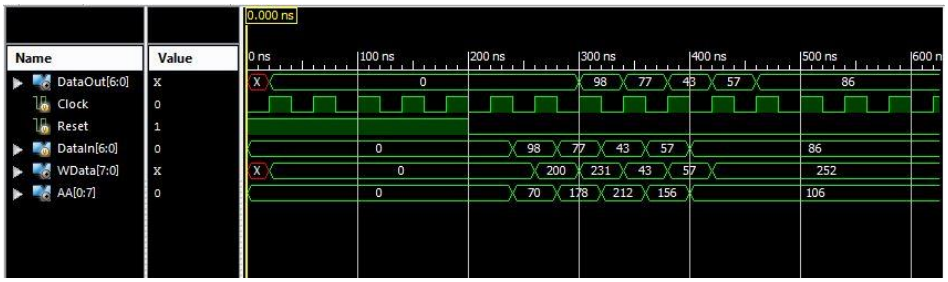

Fig 5. Encoder output

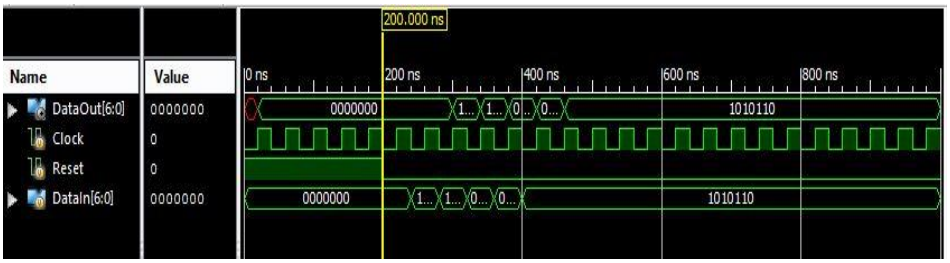

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Fig 6. Decoder output

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Timing constraint: Default OFFSET OUT AFTER for Clock 'Clock'
  Total number of paths / destination ports: 7 / 7
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Offset:              4.394ns (Levels of Logic = 1)
  Source:            DE/DataOut_6 (FF)
  Destination:       DataOut<6> (PAD)
  Source Clock:      Clock rising

  Data Path: DE/DataOut_6 to DataOut<6>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             3   0.591   0.531  DE/DataOut_6 (DE/DataOut_6)
     OBUF:I->O                3.272          DataOut_6_OBUF (DataOut<6>)
    ----------------------------------------
    Total                     4.394ns (3.863ns logic, 0.531ns route)
                                      (87.9% logic, 12.1% route)

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Fig 7. Encoder output

V. CONCLUSION

In this work, we presented the ACDMA NoC crossbar to enable parallel transmission of multi-bit data packets on a single CDMA channel. The overhead of channel replication is mitigated which results in up to 60.5% area and 55% power savings with 124% improvement in throughput per area compared to the conventional CDMA crossbar. As a future work, we plan to build and evaluate a full ACDMA-based NoC under different workloads and routing protocols.

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