Journal of Cardiovascular Disease Research

ISSN: 0975-3583, 0976-2833 VOL12, ISSUE 9, 2021

SYMMETRICAL HALF-BRIDGE SUBMODULE MULTILEVEL CONVERTERS: MODELLING AND DESIGN WITH SENSORLESS VOLTAGE BALANCE

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ABSTRACT−
Scalability and modularity are advantages of H-bridge-based multilevel converters, such as cascaded H-bridge converters. Nevertheless, they have higher conduction losses than their half-bridge-based counterparts due to the fact that each submodule requires two switches to conduct simultaneously in order to provide a current path. They also suffer from the complexity and costs associated with a high number of semiconductor switches, along with their drivers and peripheral circuits. This work presents revolutionary multilevel converters with symmetrical half-bridge submodules to minimize conduction losses and the number of active switch semiconductors. The symmetrical half-bridge submodule is simple, has fewer switches, and a bipolar voltage output. Additionally, using diodes and submodule parallelization, this study suggests a sensorless voltage balancing system that effectively eliminates capacitor voltage mismatch issues. This design can save dc capacitances by significantly reducing ripples in capacitor voltage, especially when multiple submodules are involved. Ultimately, the superiority of the suggested voltage balance scheme and multilayer converters is validated by modeling and experimental findings.

Index terms: sensorless voltage balance, modular multilevel converter (MMC), half-bridge, cascaded H-bridge (CHB), multilevel converter.

I.INTRODUCTION

The development of multilevel converters promises to advance high-voltage dc (HVdc) and ac (HVac) transmissions [1], medium voltage motor drive (e.g., automotive propulsion and marine drive) [2], renewable generation [3], power quality enhancement [4], medical applications such as pulse synthesizers for noninvasive magnetic brain stimulation [5], energy storage integration, and electric vehicles [6]. Attractive features of multilevel converters include the use of low-voltage semiconductors for high-voltage treatments, high power quality, the possibility of removing passive filters [7], low electromagnetic interference noises (due to reduced voltage and current changing rates), high reliability and redundancy, and diminished common mode problems [6]. Despite these identified advantages, multilevel converters are burdened by the complexity and costs associated with large amounts of active and passive components. Such shortcomings push forward the research of simpler multilevel converters [8].

To date, cascaded bridge, diode-clamped, and flying capacitor converters are proving to be appealing choices [9−11]. Cascaded bridge converters stand out among them due mostly to the removal of additional diodes or balancing capacitors, modularity, and scalability. Assembling cascaded bridge converters into larger structures, one can readily derive the wellknown modular multilevel converter (MMC) [12]. Recent years witness continuing progress in the commercialization and development of MMCs [13]. Since its inception, the research on the submodules of cascaded bridge converters and MMCs continues its upward trend [13−15]. This is understandable, as submodules greatly impact the cost and performance of multilevel power conversion systems. For selection of submodules, the H-bridge circuit shown in Fig. 1(a) is well-proven. It enjoys the benefits of a bipolar voltage output, a standard structure, and short-circuit protection in MMCs [13]. However, H-bridge-based multilevel converters suffer from the complexity and costs associated with a large count of semiconductor switches paired with their drivers and peripheral circuits, which are the common drawbacks of multilevel converters. Another key concern appears to be higher conduction losses as compared to half-bridge-based counterparts, as two switches in each submodule must conduct to form a current path. Aiming to address the above-mentioned concerns, the asymmetrical half-bridge submodule depicted in Fig. 1(a) quickly finds its widespread applications in half-bridge and three-phase MMCs [12], [16]. It saves half of switches and dramatically simplifies converter circuits. Nevertheless, this half-bridge submodule allows only a unipolar voltage output, i.e., the dc voltage or zero, thereby failing to operate in cascaded bridge converters and single-phase H-bridge MMCs, where bipolar voltage outputs cannot simply be

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achieved via the voltage differences between lower and upper arms [14], [17]. As such, H-bridge submodules continue to dominate the application of cascaded bridge converters so that the cascaded H-bridge (CHB) becomes a standard terminology [3], [18]. Novel submodules, such as flying capacitor [14], neutralpoint-clamped (NPC) [15], clamp-double [19], double-zero [13], mixed half-bridge and H-bridge [15], and double Hbridge submodules [20], were proposed for various purposes, e.g., the increment of voltage levels, short-circuit protection, and parallel connectivity. Although some of these submodules proved to be attractive, they are more complicated than the Hbridge submodule. In fact, the symmetrical half-bridge submodule illustrated in Fig. 1(b) is a promising alternative to the H-bridge submodule. The benefits of symmetrical half-bridge submodules comprise a marriage of bipolar voltage outputs (featured by H-bridge submodules) and reduced switch counts and conduction losses (possessed by half-bridge submodules). Notably, symmetrical half-bridge converters remain an active area of ongoing research. Their candidate applications include active rectifiers [21], active power filters (APFs) [22], power decoupling circuits [23], unified power quality conditioners (UPQCs) [24], linear compressors [25], etc. Although the symmetrical halfbridge circuit presents a clear advantage from the implementation point of view, it is historically been of little interest in multilevel converters. One major barrier narrowing the application of symmetrical half-bridge submodules to single converters refers to the imbalance of upper and lower capacitor voltages, as will be detailed in Section IV. After removing this barrier, one can reap the advantages of symmetrical halfbridge submodules in multilevel converters. This paper proposes novel multilevel converters with symmetrical half-bridge submodules and sensorless voltage balance.

II.PHASE LOCKED LOOP

A phase-locked loop or phase lock loop (PLL) is a control system that tries to generate an output signal whose phase is related to the phase of the input "reference" signal. It is an electronic circuit consisting of a variable frequency oscillator and a phase detector that compares the phase of the signal derived from the oscillator to an input signal. The signal from the phase detector is used to control the oscillator in a feedback loop. The circuit compares the phase of the input signal with the phase of a signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched.

Frequency is the derivative of phase. Keeping the input and output phase in lock step implies keeping the input and output frequencies in lock step. Consequently, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. The former property is used for demodulation, and the latter property is used for indirect frequency synthesis.

Phase-locked loops are widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz

III. MULTI LEVEL INVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC) the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high power electronic oscillator. It is so named because early mechanical AC to DC converters were made to work in reverse, and thus were "inverted", to convert DC to AC.

3.1Cascaded H-Bridges inverter

A single phase structure of an m-level cascaded inverter is illustrated in Figure 3.1. Each separate DC source (SDCS) is connected to a single phase full bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The AC outputs of each of the different full bridge inverter

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levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate DC sources. An example phase voltage waveform for an 11 level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 3.2. The phase voltage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$$

…

For a stepped waveform such as the one depicted in Figure 4.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \frac{\sin(n\omega t)}{n}, \ where\ n = 1,3,5,7 \ldots \quad \ldots$$

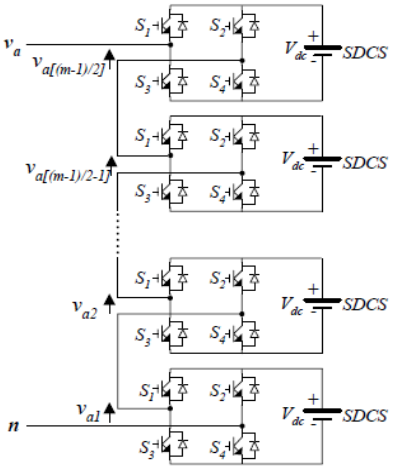

Fig1.Single-phase structure of a multilevel cascaded H-bridges inverter

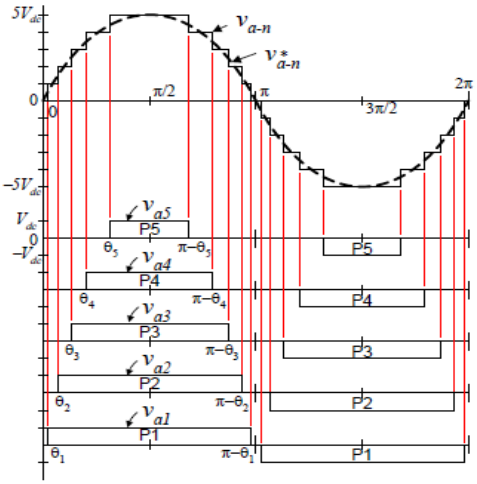

Fig2. Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources.

IV.PROJECT DISCRIPTION AND CONTROL DESIGN

FUNDAMENTAL OPERATING PRINCIPLES OF CHB CONVERTERS AND MMCS

This section reviews the basic operating philosophy of existing CHB converters and MMCs. It aims to lay the groundwork for the comparison analyses covered in the next section. For demonstration, Fig. 2 illustrates the schematic diagram of CHB converters or H-bridge-based MMC arms. As noticed, the CHB converter consists of n (n represents a positive integer) H-bridge submodules with their output terminals connected in series. Normally, H-bridge submodules convert their dc terminal voltages vdcx (x = 1, 2, … , or n) into ac terminal voltages through the operation of semiconductor switches. However, it is also possible that multilevel converters output dc voltages [14]. Without loss of generality, we denote the output voltages of individual submodules as vacx. By means of series connection, the individual submodule voltages vacx are added together, forming an overall output voltage vac. This overall voltage vac can be much greater than the individual dc-link voltages vdcx, and thereby allowing the low-voltage semiconductor switches, which are subject to dc voltage stresses, to be suitable for high-voltage applications. In terms of versatility, CHB converters are easily scaled according to the requirement of vac via the change of submodule numbers. Moreover, as all submodules are identical, CHB converters benefit from modularity. As compared to diodeclamped or flying capacitor converters, CHB converters feature

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no additional diode or balancing capacitor [2]. In addition, note that either capacitors or batteries can be used in the dc side, their major control difference lies in the regulation of capacitor voltages. In this sense, the capacitors fed by frontend rectifiers are similar to batteries [26]. In the output side (or ac side), either a power grid or an electric load may appear dependent on operating conditions [4], [26]. CHB converters are essentially the arms of H-bridge-based MMCs [17]. To generalize the concept, MMCs are multilevel converters that replace the individual active switches of typical two-level converters, such as symmetrical half-bridge, Hbridge, and three-phase-bridge converters, with cascadedbridge converters. Referring to Fig. 1(b), one can infer that the half-bridge MMC is derived by replacing the two active switches of the symmetrical half-bridge circuit with two cascaded-bridge converters [12]. There are two important properties of MMCs. One refers to the micro topology or the submodule circuit. The other is related to the macro topology or the basic two-level circuit in support of MMCs [6]. To differentiate these two properties, we use the prefix "half-bridge" to represent basic two-level circuits and the prefix "half-bridge-based" for submodule topologies. Although MMCs allow very flexible operations, they are determined by basic circuits and cascaded-bridge converters, which in turn depend on submodules. As such, the research interest on submodules maintains high [15]. One notable example is the asymmetrical half-bridge submodule shown in Fig. 1(a). Due to their size, cost, and efficiency benefits, asymmetrical half-bridge submodules have been the top option in commercial MMCs for HVDC applications until very recently H-bridge-based MMCs appear. However, the asymmetrical half-bridge submodule features unipolar voltage output and cannot continue to transfer power during dc side short circuits. Therefore, they are limited in their applications.

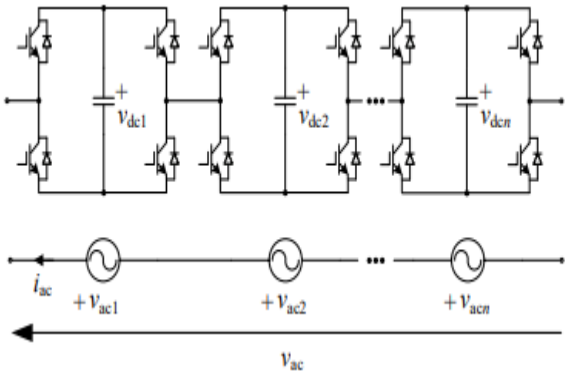

Fig3: Schematic of CHB converters or H-bridge-based MMC arms

PROPOSED MULTILEVEL CONVERTERS WITH SYMMETRICAL HALF-BRIDGE SUBMODULES

This section focuses on the principles of the proposed multilevel converters with symmetrical half-bridge submodules. Meanwhile, the benefits of half-bridge submodules are highlighted through comparisons with H-bridge submodules. A. Operating Principles of the Proposed Multilevel Converters Recapping that the asymmetrical half-bridge submodule in Fig. 1(a) simplifies MMC circuits at the expense of unipolar outputs, one can further imagine the use of symmetrical halfbridge submodules in Fig. 1(b), whose basic principle is explained as follows. With the upper switch turned on and the lower switch off, the symmetrical half-bridge submodule yields a positive voltage, i.e., the upper capacitor voltage. Alternatively, a negative output or lower capacitor voltage is expected. Combining these two operating modes, the symmetrical half-bridge submodule allows a bipolar voltage output with a simple structure. The proposed cascaded bridge converter or MMC arm with symmetrical half-bridge submodules is shown schematically in Fig. 3. Once again, the overall output vac is contributed by individual submodule outputs vacx (x = 1, 2, … , or n). In this regard, the proposed cascaded bridge and CHB converters share the same basic operating principles. Next, the benefits of the proposed converters will be disclosed. B. Cost Analysis Before conducting a detailed cost analysis, we first analyze the requirement of passive and active components in cascaded bridge converters. Returning to Fig. 2, one can note that a CHB converter with n submodules necessitates 4n active switches, e.g., insulated-gate bipolar transistors (IGBTs) or metal-oxide semiconductor field-effect transistors (MOSFETs), in combination with n dc capacitors. Proceeding to Fig. 3, the proposed cascaded bridge converter with n submodules obviously requires 2n active switches and 2n dc capacitors. In comparison, the proposed converter saves half of switches at the expense of more dc capacitors. Nevertheless, when applied to renewable energy generation, the additional dc capacitors of the proposed converter allow the integration and independent control of more renewable energy resources. If batteries are used in replacement of dc capacitors, the proposed converter allows a finer balance of battery cells. In summary, Table I lists the component comparison results, where the on-state switch refers to the switch that conducts currents, which will be discussed later. It is important to remember that the above comparison holds valid for singlephase converters. In the case of three-phase converters, the numbers of switches,

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drivers, and dc sources triple, but so do the savings. Despite the saving with respect to the number of semiconductors, the half-bridge submodule stresses its active switches with double the dc voltages (i.e., vdcxu + vdcxd = 2vdcx = 2Vdc) as compared to H-bridge submodules. For a fair comparison, switch pairs with twice voltage rating differences and similar other features (e.g., technologies, switching frequency ranges, and current ratings) are documented in Tables II−IV [27−29], where the comparisons cover major active switches, including IGBTs, Si MOSFETs, and gallium nitride (GaN) FETs. It should be mentioned that silicon carbide (SiC) MOSFETs are excluded, because they are currently marketed for one narrow voltage band [30]. By examination of Tables II−IV, the prices of high-voltage switches are always lower than twice the prices of their low-voltage counterparts. In several cases, the price differences between switch pairs are relatively minor or even

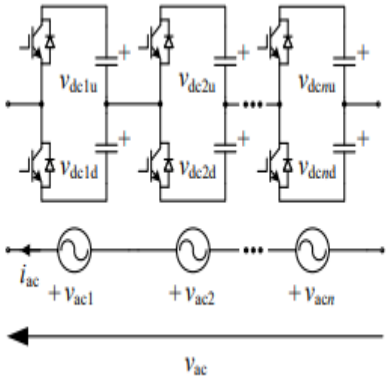

Fig4: Schematic of the proposed cascaded bridge converters or MMC arms with symmetrical half-bridge submodules

CHALLENGES AND SOLUTIONS OF CAPACITOR VOLTAGE BALANCE

This section points out the capacitor voltage balance challenge faced by the proposed multilevel converters with symmetrical half-bridge submodules. As a solution, it introduces a novel and effective voltage balance scheme that equalizes capacitor voltages and reduces their ripples. A. Voltage Balance Challenge The mismatch between the upper and lower capacitor voltages (see vdcxu and vdcxd in Fig. 3) is an issue peculiar to symmetrical half-bridge submodules and converters. This issue may beget undesirable over-modulation, current distortion, or malfunction of power converters. Capacitance tolerances, dc voltage sensor offsets, and ac current sensor offsets are typical factors causing capacitor voltage imbalances [21]. The injection of a dc component into ac current references is a straightforward solution to the voltage balance issue of half-bridge converters [21], [22], [25]. This solution adds a positive dc component in the output current when the upper capacitor voltage exceeds the lower one. In this way, the discharge and charge times of the upper and lower capacitors increase, respectively, collectively leading to the balance of capacitor voltages. Unfortunately, the aforesaid solution is not applicable to half-bridge-based multilevel converters. To justify this statement, Fig. 9 displays the control block diagram of grid-tied cascaded-bridge converters with symmetrical half-bridge submodules, where the input signals vgrid, vdc_ref, iq_ref represent the grid voltage, capacitor voltage reference, and reactive current reference, respectively. PLL refers to the abbreviation of the phase-locked-loop. GPI(s), GPR(s), GFil_1(s), and GFil_2(s) stand for the transfer functions of proportional integral (PI) controllers, proportional resonant (PR) controllers, notch filters at the fundamental frequency, and those at the 2nd harmonic, respectively. The output signals d1, …, dn−1, and dn, are fed to the pulse width modulators (PWMs) of individual submodules. As shown in Fig. 9, the overall control block diagram consists of n dc voltage, one current, and one voltage balance control blocks. As the modulation of symmetrical half-bridge and (bipolar modulated) H-bridge submodules are identical, the control block diagram in Fig. 9 largely follows that of singlephase CHB converters except for the voltage balance control [3]. This PWM-based control scheme allows independent dc voltage control. The dc voltage blocks target at the regulation of the capacitor voltage sum in each half-bridge submodule.

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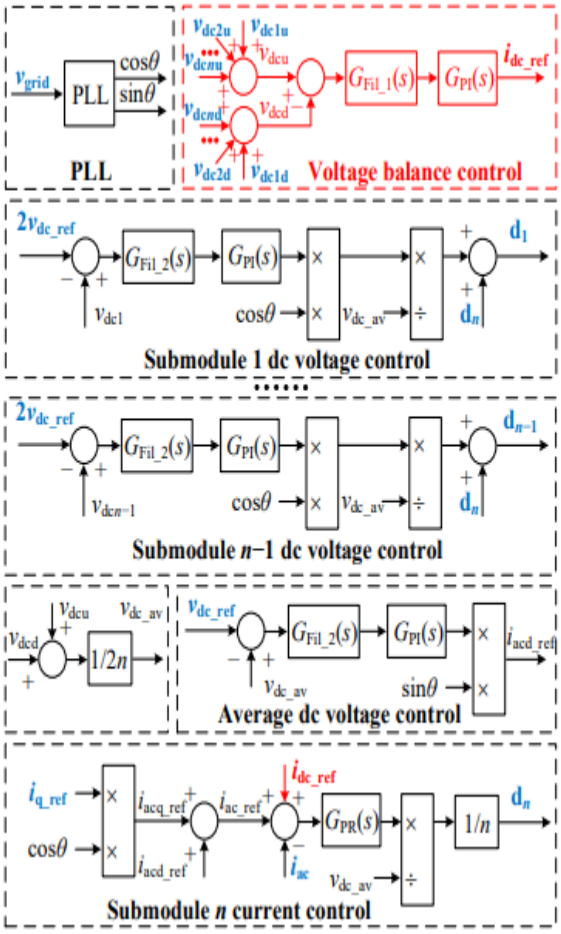

Fig5: Control block diagram of grid-tied cascaded-bridge converters with symmetrical half-bridge submodules.

The current block regulates the grid-injected current. Elevated attention should be paid to the voltage balance block, where the error between the upper and lower capacitor voltage sums, i.e., vdcu−vdcd, is regulated by a PI controller, whose output idc_ref subsequently becomes the dc current reference in the current block. This voltage balance control removes voltage imbalances in half-bridge converters [25]. However, it fails to clear the voltage difference in every submodule of multilevel converters, as the current control features only one degree of freedom. Therefore, the voltage balance issue of half-bridgebased multilevel converters remains unsolved. For validation, Figs. 10 and 11 illustrate Matlab simulation results of voltage balance control in grid-tied half-bridge converters and cascaded-bridge converters, where the system and control parameters are listed in Tables VI and VII, respectively. In Table VII, the control gains of inner-current and outervoltage loops are tuned following the same design procedure as those of single-phase two-level grid-tied converters and half-bridge converters, as detailed in [22], [37], [38]. Except for the grid voltages (110 Vrms in Fig. 10), the simulation parameters of the two cases are identical. Initially, the upper capacitor voltage in one submodule is intentionally designed to be 50 V greater than the nominal dc voltage 200 V, opposite to the corresponding lower one, while the remaining submodules are with nominal voltages. After the activation of voltage balance control, the half-bridge converter achieves a satisfactory voltage balance. In contrast, the cascaded-bridge converter only equalizes voltage sums, i.e., vdc1u+vdc2u+vdc3u = vdc1d+vdc2d+vdc3d, rather than individual voltages. B. Proposed Voltage Balance Scheme Fig. 12 presents the proposed voltage balance scheme, where each symmetrical half-bridge submodule employs two additional diodes. Note that the two diodes of the rightmost submodule can be removed for simplicity. These additional diodes DS1u, DS1d, DS2u, and DS2d enable a sensorless balance of all capacitor voltages through submodule parallelization. For instance, the upper capacitor of the second submodule is in parallel with the lower capacitor of the first submodule, when TS2u is turned on, and vdc2u is greater than vdc1d. This parallel connection nulls the difference between vdc2u and vdc1d. Similarly, the voltage mismatch between vdc1u and vdc2d is cleared through DS1u and TS2d. It is worth mentioning that the on-state voltage drops of semiconductors are ignored here. In addition, the idea of voltage balancing via submodule parallelization and its related analysis have been investigated with other MMC topologies [6],

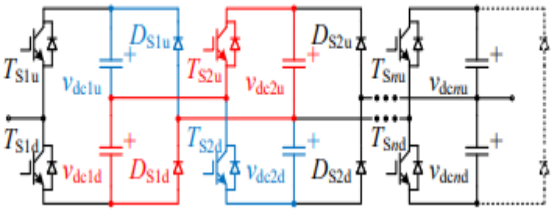

Fig6: Schematic of the cascaded bridge converters or MMC arms with symmetrical half-bridge submodules and sensorless voltage balance.

High reliability and sensorless operation are two important benefits of the proposed voltage balance scheme. A further advantage lies in the reduction of voltage ripples. To analyze this, Fig. 13 illustrates the four basic operating modes of the proposed cascaded bridge converters with symmetrical halfbridge submodules and voltage balance scheme. These operating modes are drawn based on several assumptions, including the ignorance of on-state

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voltage drops, equivalent series resistors, and the conditions where diodes cannot conduct. Let us first focus on the right-hand-side submodule. If its lower switch TS2d turns on [see Fig. 13(a) and (b)], the relevant capacitor Cdc2d will be connected in parallel with the upper capacitor Cdc1u of the left-hand-side submodule. Furthermore, the two capacitors will continue to parallelize submodules leftwards if Ts1u conducts, as shown in Fig. 13(a). Alternatively, Fig. 13(b) indicates that Cdc2d and Cdc1u will not parallelize leftwards if Ts1d conducts. Similarly, Fig. 13(c) and (d) demonstrate the cases where TS2u turns on. It can be concluded from the above discussion that the number of paralleled capacitors is influenced by the operating modes of the proposed multilevel converter, which in turn depends on its ac voltage reference. In the most favorable case, all the diagonal capacitors are in parallel, and the resultant current following through each capacitor reduces by a factor of n. Correspondingly, the voltage ripple and dc capacitance requirement also decrease by a factor of n. The above analysis is well applicable if the ac voltage is relatively low when the ac current reaches its peak, such as in STATCOMs. According to the circuit theory, the sudden parallelization of two voltage sources (like capacitors) with different voltages is not allowed. However, practical capacitors and switches feature equivalent series resistors (ESRs) and inductors, which attenuate current spikes [6]. Moreover, real switches exhibit forward voltage drops, which are also beneficial for surge current limitations. Detailed analysis of power losses due to parallelization can be found in [6] and [20]. One obvious drawback of the proposed voltage balance scheme refers to the additional cost brought by diodes. Fortunately, diodes are generally much cheaper than the active switches under similar power ratings, as proved by Table VIII [42]. Moreover, diodes operate without drivers or peripheral circuits, and hence save the related costs. More importantly, they deserve the credit for reducing dc voltage ripples and capacitances, and the saving grows as the number of submodules increases. Thus, half-bridge-based multilevel converters can be economically desirable in terms of both passive capacitors and semiconductors.

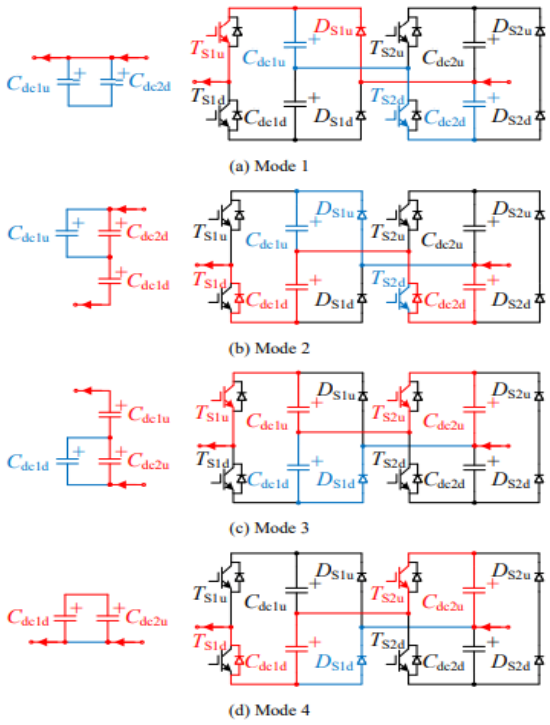

Fig7: Operating modes of the cascaded bridge converters or MMC arms with symmetrical half-bridge submodules and sensorless voltage balance.

V.SIMULATION RESULTS:

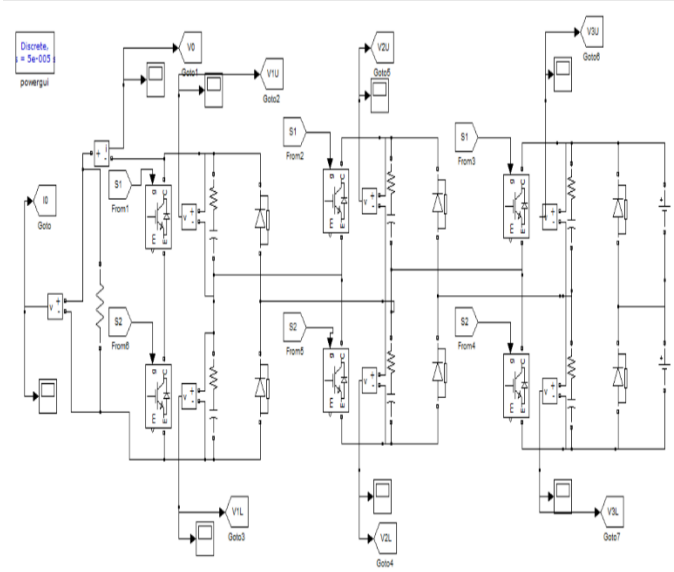

Fig8: Proposed simulation diagram

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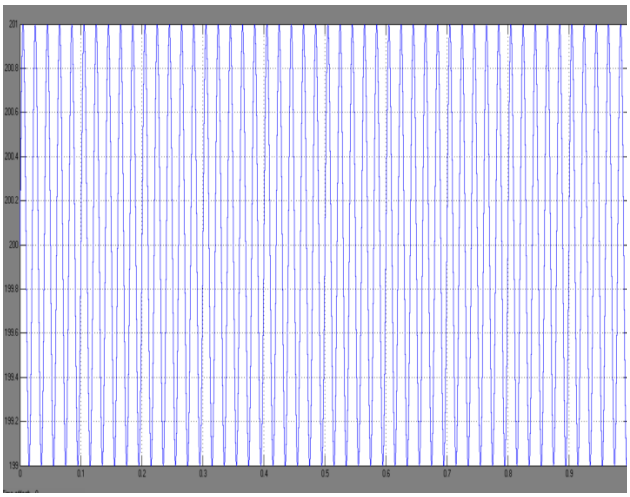

Fig9:V1u

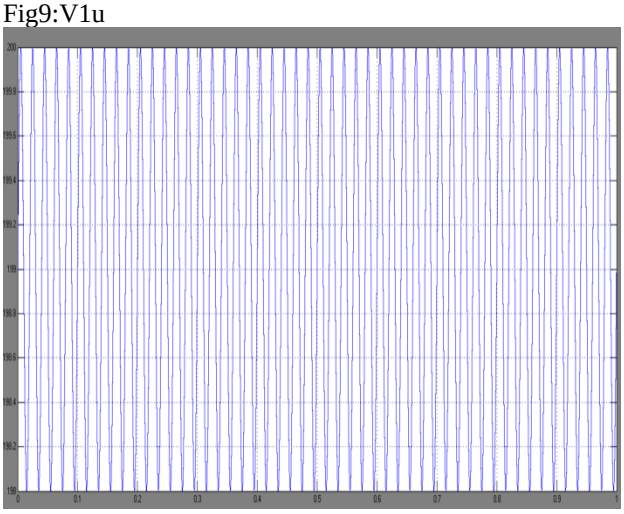

Fig10: V1l

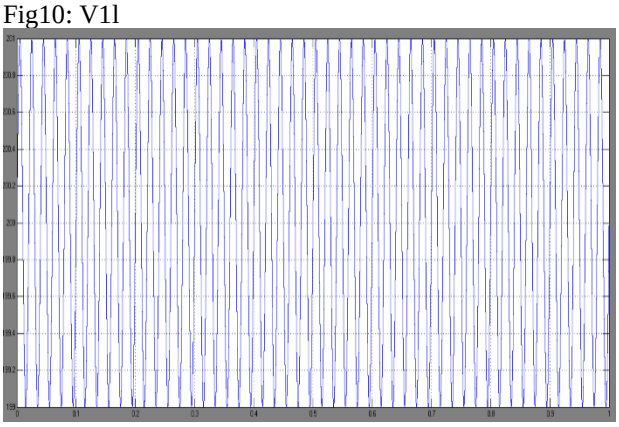

Fig11: V2u

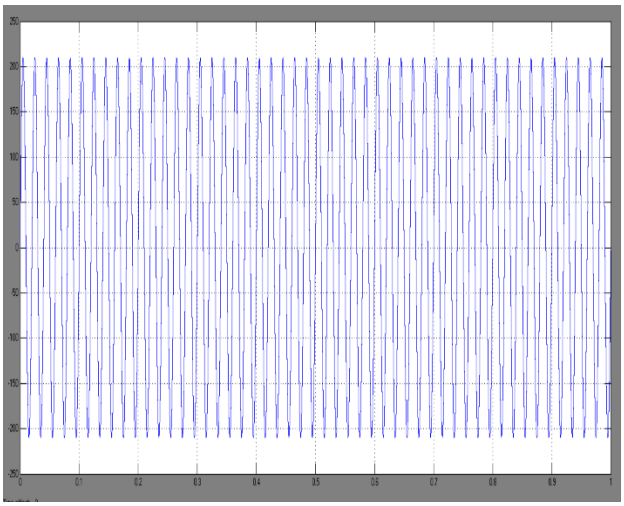

Fig12:V0

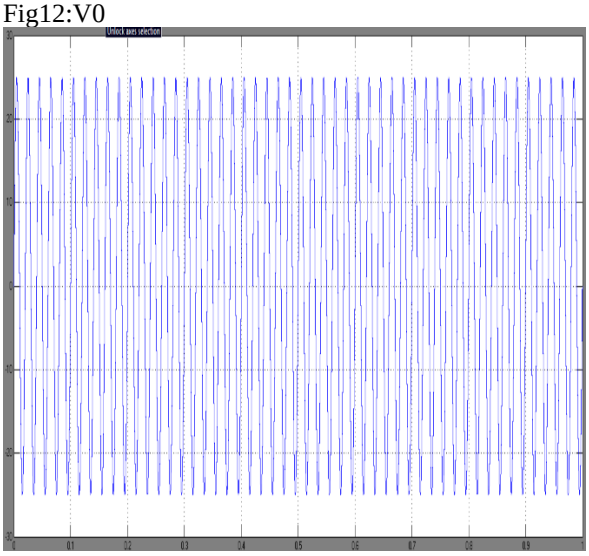

Fig13:Io

VI.CONCLUSIONS

A novel multilevel converter family with symmetrical half-bridge submodules has been proposed in this paper. This series provides excellent simplicity and reliability together with minimal prices and conduction losses. The proposed voltage balance solution offers additional incentives by eliminating voltage sensors and conserving DC capacitances with the use of diodes. The suggested voltage balancing approach is especially useful in scenarios when a large number of multilevel converter submodules are anticipated. The voltage balance system and suggested multilayer converters are finally simulated, and the results demonstrate good agreement with the theoretical analysis.

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