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Implementation of Transient Current Testing for Faults in SRAM

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Abstract:

In recent years, as memory devices have risen in popularity, a higher quantity of memory has been packed into each chip, and fierce market competition has upped the quality standards that are expected of the memories that are produced. The notion that failure analysis and device testing methodologies are becoming increasingly important as a result of the rising demand for dependability has been emphasised repeatedly. It has been more popular to study and research memory devices in recent years, particularly in the context of novel failure models, fault detection methodologies, and new memory architectures that have all been developed and implemented. A direct effect of this experience is that the March test is now frequently used to identify and avoid similar problems from occurring in the future. The organisation believes that some vulnerabilities in SRAM cells may go undetected during the normal March testing. In order to determine whether or not there are defects in the CMOS SRAM, a time-consuming procedure has been implemented. It is as a result of this decision that the most recent testing process is selected for usage. As part of this research effort, IDDT is being used to test for faults and issues in CMOS SRAM cells, and it is also being used to test for flaws and issues in CMOS SRAM cells as part of a separate study of the same name. In either case, a transient current pulse generated during a transition write operation or a transition read operation may be monitored for system failures, allowing them to be discovered and remedied. For the purpose of detecting and measuring the transient current pulse, it is required to design a circuit for monitoring current.SRAM, memory testing, the March algorithm, the IDDT, and the current sensor circuit are just a few of the terms that appear in this document.

I. INTRODUCTION

In order to get higher performance in order to meet the demands of today's and tomorrow's applications, today's systems on chips (SoCs) are changing from being dominated by logic to being dominated by memory. [1] [2] Memories are expected to account for 90 percent of all semiconductor chip area by 2013, according to the International Technology Roadmap for Semiconductors (ITRS), with static random access memory (SRAM) accounting for the vast

ISSN:0975-3583,0976-2833 VOL10,ISSUE04,2019

majority of this space. This means that the yield of the memory has a significant impact on the total yield of the SoC. Figure 1: Memory yield. Figure 1 shows a diagram of a compass. The concept of memory yield is introduced. Devices whose sizes have been drastically reduced are witnessing an increase in the number of failures they experience. Because it has a higher number of hardware components than other circuits, the memory unit is frequently the component in a computer system that has the lowest level of dependability, according to industry standards. The SRAM memory cell has the highest density when compared to other logic circuits because of its high density; yet, due of its high density, it is also the most prone to failure when compared to other logic circuits. Aside from that, changes in the manufacturing process have an influence on the functioning of memory, and as technology advances, these inconsistencies are becoming more prevalent across the board in the industry.

It follows that the test cost of memory will have a significant influence on the test cost of SOCs in this case as a result of this. The cost of memory during the exam is depicted in Figure 1. It is possible to generate less product when there are faults in the memory because the presence of errors in the memory reduces the quantity of product that can be produced. In the case of mission-critical systems, the use of these methodologies has the potential to result in the failure of the system under discussion. Consequently, it is vital to use suitable testing processes in order to reduce costs while preserving efficiency, consequently improving the overall quality of the product produced. A variety of fault models are employed in SRAM testing to discover potential difficulties. These include stuck-at faults, transition faults, and coupling faults, to name a few. As proved by the March tests [3] and [4], it has been routinely utilised to find these flaws in order to expose them to the public. These detection procedures, on the other hand, need a large investment of time and resources. [5] [6] There have been a number of different approaches of inductively inducing quiescent current testing, as well as combinations of these approaches [7, 8] that have been employed. It is possible that the IDDQ will fail to identify certain flaws in SRAM cells, which is a positive in this specific circumstance. An open defect detection approach based on transient current testing is employed in this study to discover open faults in CMOS SRAM cells. Using a transient current testing approach, which was employed in this study to discover open faults, this methodology is based on the findings of the study. It is feasible to discover errors while executing a written or read operation by monitoring a transient current pulse that is generated during the writing or reading activity.

II. BACKGROUND

A. SRAM Cell

A repeating structure improves the efficiency of transient current testing since it increases the number of tests that can be run at the same time. It is as a result of this that this method is appropriate for use with SRAM memory cells. It is believed that 6T CMOS SRAM cells account for more than 70% of all SRAM cells in modern SOCs and microprocessors [7], making them

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the most widely used SRAM cells in the industry. Consequently, it is critical to remember the 6T CMOS cell represented in Figure 1 while designing CMOS devices. It is possible to perform read and write operations on the cell because of the use of the NMOS transistors M5 and M6, which were particularly built for this purpose. In addition to two cross-coupled inverters, which are created by transistor complementary pairs M1-M3 and M2-M4, the cell contains two access transistors M5 and M6, which are typically NMOS transistors and are responsible for ensuring that read and write operations in the cell are successful. M5 and M6 are typically NMOS transistors and are responsible for ensuring that read and write operations in the cell are successful. In addition, the cell has two access transistors M5, which are generally NMOS transistors, as well as a cell-bus interface.

There are two types of write operations on SRAMs: transition writing and non-transition writing. Both types of write operations are described in detail below. Among SRAMs, transition writing is the most often encountered style of writing. The transition writing style, which is explained in further detail below, is the most prevalent type of writing. When the transition writing procedure is done, there will be a brief increase in the amount of current flowing from the power source to the earth ground. If either a transient current is recorded during a non-transition write or no transient current is measured during a transition write, it is possible to conclude that the cell has a defect. It is also crucial to note that the presence of different faults results in different peaks of transient current, which may be monitored in order to anticipate the development of faults, which is another key feature to remember.

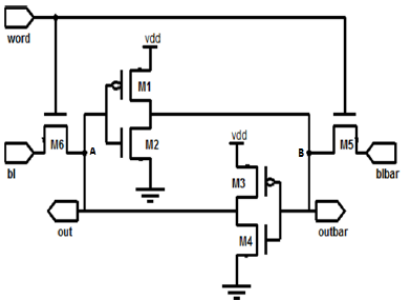


Figure 1: 6T CMOS SRAM cell

B. Faults introduced

As a result of the launch, a number of problems were introduced into the environment.

A problem or mistake in the logical or electrical architecture of the SRAM can develop for a variety of reasons, including manufacturing mistakes, component ageing or destruction (for example, as a consequence of radiation exposure), or process variations. Flaws in a product that were not intended to be there at the time of manufacture but were discovered after the product has been completed are referred to as manufacturing faults. No matter how meticulously

ISSN:0975-3583,0976-2833 VOL10,ISSUE04,2019

designers and manufacturers work, a manufacturing error is nearly guaranteed to occur despite their best efforts.

As a result of the high size of SRAM, it is not practical to physically inspect the memory in its entirety during testing. So the comparison of logical behaviour between memories that contain errors and memories that are in excellent condition serves as the foundation for the testing technique described above. To understand why some memories fail and others do not, it is necessary to model physical failure mechanisms as logic fault models. For example, it is necessary to compare the logical behaviour of faulty memories to the logical behaviour of good memories in order to determine why some memories fail and others do not. The SRAM will be held responsible for both an open and a bridging fault if any of these errors causes the memory system to become non-responsive.

In order to determine the impact of resistive open flaws on SRAM core-cell performance, it is common practise to introduce faults into the circuit itself and then observe the results of the investigation. This is done in [8] and [9] to determine the impact of resistive open flaws on SRAM core-cell performance. This has occurred as a result of the fact that the investigation's findings are more reliable. Only one defect should be mentioned in each analysis for the purpose of simplicity, and this will help to keep things as simple as possible throughout the procedure. Due to the fact that the development of many flaws in a circuit with just six transistors is extremely rare, it is not required to address this issue at the time of design or construction. A fault injection into the SRAM core-cell happens during the device's manufacturing process, as seen in Figure 2. The injection of the problem is marked in red. It is typical to locate resistive open flaws in a circuit around the connections since this is the area where they are most likely to cause problems in the first place. This part describes how, because of the structure's symmetry, it is feasible to perform a detailed analysis of the resistive-open flaws inside the core-cell structure at the six locations mentioned in this section.

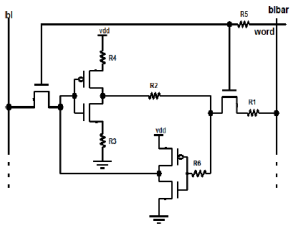


Figure 2: Open faults in SRAM

According to the real-world industrial core cell arrangement, the [10] and [11] Resistance Bridges have been placed in the appropriate locations on the circuit board. Several more factors, such as supply voltage, memory size, and temperature settings, were taken into consideration during the examination of each problem, among them. For the sake of demonstration, a resistive-bridging fault (R7 to R11) has been inserted in various locations around the core-cell in Figure 3 to show how they function. It is feasible to reveal resistive-bridge arrangements in a symmetrical

ISSN:0975-3583,0976-2833 VOL10,ISSUE04,2019

design by looking at the resistances R8 through R11 of the design. The use of R7 makes it difficult to create a symmetrical defect since it is a fault between the internal nodes of the core-cell, and it is not symmetrical in the first place.

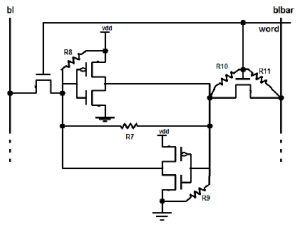


Figure 3: Bridging faults in SRAM

Based on how they interfere with the operation of SRAM, bridging faults may be divided into two types: internal and external. The first type of faults is bridging flaws, which are distinguished by the following characteristics: This set of cells may exhibit abnormal behaviour when read and/or write operations are performed on the data storage medium in which it is stored if a failure occurs in this group of cells. Any of the defects listed in this category may cause the core-cell to behave abnormally when read and/or write operations are performed on it during read and/or write operations. In contrast to other forms of mistakes, Group 1 errors are distinguished by the presence of erroneous behaviour inside a single cell. Because they are only expected to have an impact on the electric nodes within the core-cell, these defects are classed as being in Group 1 of the classification system. The R7, R8, and R9 radial arteries are all members of Group 1.

In Group 2, faults can have an influence on the behaviour of the faulty core-cell, but they can also have an impact on the behaviour of the other non-defective core-cells in the array if the array contains many defects. As a result, faults in Group 1 have no effect on the behaviour of the malfunctioning core-cell, and as a result, they are categorised as noncritical errors. Defects in Group 2 can present themselves in a variety of ways, one of which is the presence of double-cell faulty behaviour. These nodes are included in Group 2 because the faults in R10 and R11 have the ability to significantly influence both BL and WL nodes, which is why they are included in Group 2. However, rather than using only one damaged core-cell, as had previously been proposed, a more precise model of the SRAM array is currently being researched. Because current sources properly model leakage effects and, as a result, lower simulation durations, current sources have been used to replace the vast majority of core cells in order to accelerate simulations.

As a result, it is feasible to produce a failure in an SRAM by inserting any of the resistances listed above into the device. This is a list of the resistance values that were used in the experiment, which can be found in Table I of this document. Furthermore, the word "particular" denotes the sort of specific fault that is being discussed in this context.

ISSN:0975-3583,0976-2833 VOL10,ISSUE04,2019

TABLE I RESISTANCE INTRODUCED IN SRAM TO MODEL OPEN FAULTS

Resistance	Resistance Value(Ω)	Nature of fault	Fault model
R1	1MΩ	Open defect 1	TF
R2	1MΩ	Open defect 2	DRF
R3	1MΩ	Open defect 3	S-a-1
R4	1MΩ	Open defect 4	DRF
R5	1MΩ	Open defect 5	SOF
R6	1MΩ	Open defect 6	DRF
R7	10Ω	Bridging defect 1	SAF
R8	10Ω	Bridging defect 2	S-a-1
R9	10Ω	Bridging defect 3	S-a-0
R10	10Ω	Bridging defect 4	CF
R11	10Ω	Bridging defect 5	CF

Following that, in the following portion of this article, we will go into further detail about the logic failure models that have been established for SRAM. In the model, there are five basic types of functional failures: the stuck-at fault (SAF), the transition fault (TF), the stuck–open fault (SOF), the coupling fault (CF), and the data retention fault. The stuck–at fault (SAF) is the most common type of functional failure. The stuck–at–fault (SAF) form of functional failure is the most prevalent type of failure (DRF). It is the most common sort of functional mistake, accounting for around one-third of all cases (DRF).

A memory cell that always has the same value, either zero or one, and that fails to write the other value while the cell has either zero or one value is referred to as a "stuck-at-fault." S-a-1 denotes that you have been stranded at the number one position, whilst S-a-0 indicates that you have been stranded at the zero position.

An example of a transition defect is a circumstance in which a memory cell successfully completes a transition in one direction but fails to successfully complete a transition in the other. A transition fault, as opposed to a regular stuck–at issue, is a type of stuck–at defect that is substantially more severe than a typical stuck–at issue. As a result of an error in the programme that produced the "stuck–open fault," it is impossible to read or write to a memory cell that has been marked as "stuck–open fault." Whenever a SOF is present in a cell, no read or write operations are permitted on that specific cell.

The phrase "coupling error" refers to input/output mistakes that occur when the contents of one memory cell are influenced by the contents of another memory cell, which can occur when the contents of one memory cell are influenced by the contents of another memory cell. The phrase "coupling error" refers to the error that happens when the contents of one memory cell are influenced by the contents of another memory cell, as in the case of a memory cell whose contents have been influenced by the contents of another memory cell. Following the passage of time, a memory cell that has lost the content it previously contained is referred to as having suffered from a data retention defect.

ISSN:0975-3583,0976-2833 VOL10,ISSUE04,2019

SENSOR TECHNOLOGY AND ARCHITECTURE (PART III)

As a result, because the IDDT current [12] [13] produced by the VDDT Sensor [12] occurs in such a short period of time [12], it is difficult to recognise and analyse it. As a result of the fact that it is innately intractable by its very nature, processing the dynamic supply current with low-power technology is almost impossible. As a consequence of the adjustments that have been implemented

In accordance with [15], it is feasible to construct a strategy that involves the conversion of current to voltage and then dealing with the voltage waveform that is produced [14]. When a VDDT sensor is in use, the operation of the sensor may be observed in Figure 3. While the presence of a dynamic current in the output voltage may still be seen, the time scale has been shifted to the right. With this extra time, you may perform additional processing over the Christmas holiday season and beyond. When opposed to the March tests, which need a minimum of four write operations to identify the problem, the April test requires just two write operations to detect the problem. This is one of the various advantages of the April test. Furthermore, the examination is less expensive. The speed with which the test is carried out is critical since it has the capability of identifying the problem in a shorter period of time than other methods.

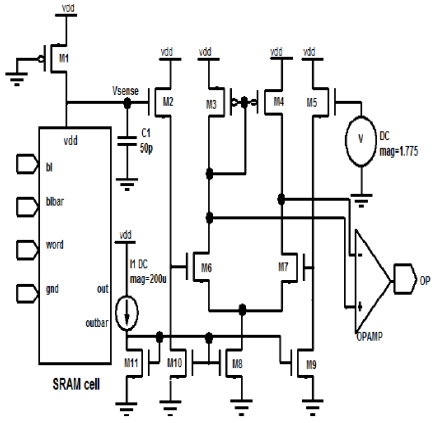


Figure 4: VDDT Sensor

In this example, the transistors M2 and M5 are used as two emitter followers, and they function under the same direct current (DC) conditions as the first transistor, M1. Compared to the other transistors in the cell, the first transistor, M1, has a voltage drop across it that is close to 0 volts when compared against the others. As a result of the fact that M1 is significantly larger in physical size than the other transistors in the cell, this occurs. Just as it is possible to regard M5's gate as connected to VDD, the gate of M2 may be considered as being connected to VDD, as can the gate of M5. The currents that flow via the M5 and M2 terminals, in addition, are virtually similar, resulting in nearly identical DC conditions for the transistors on both sides of the bridge. Because of this design on both the differential pair (M6-M7) and the differential pair, it is

ISSN:0975-3583,0976-2833 VOL10,ISSUE04,2019

guaranteed that both the differential pair (M6-M7) and the differential pair will have stable DC conditions when compared to each other. The voltage waveform indicated by the symbol C can be made longer by including a capacitor C in the circuit in order to allow for a longer period of time in the node Vsense. Therefore, while designing circuits for this application, the most important factor to consider is the greatest possible device matching. As a result, the differential amplifier's output is connected to the input of a high gain operational amplifier, which allows the transient voltage in millivolts and microvolts to be transformed into millivolts and microvolts, respectively, at its output.

The supply current required by a fault-free SRAM cell is minimal in steady state, resulting in the cell drawing near to zero static current in compared to the rest of the system while operating at steady state. This implies that a large amount of current from the power source is only required during the period in which the cell is changing its state, which occurs only during the period in which the cell is charging. Providing that this condition is met, it is feasible to establish a transient current channel between the voltage source and the ground potential. As a result of the charging and discharging of node capacitances in conjunction with the switching action, a current flow occurs that lasts only for the duration of the switching operation, which is referred to as the dynamic or transient current flow. The charging and discharging of node capacitances in conjunction with the switching action results in a current flow that lasts only for the duration of the switching operation. As a result of the charging and discharging of node capacitances in conjunction with the switching action, a current flow is created that is only active for the period of the switching operation.

The presence of this current is recognised by the pmos M1 circuit, which is in charge of detecting its presence. In the case of the voltage that was measured, the units of measurement are volts (V) (SENSE). The V range of the waveform V has several little spikes, which are most noticeable in the V region of the waveform V. (SENSE). Upon application of a brief transient voltage to the differential pair, the differential pair gets an instantaneous differential signal from the source voltage. As a result, given that differential device matching is performed correctly, it is possible to generate outputs that are basically identical at the output nodes of the differential device matching system. In order to make this connection conceivable, an operational amplifier with a high gain is used to connect the outputs of the two operational amplifiers together. Due to the fact that the voltage is in the V range, it is theoretically feasible that signal processing will be straightforward.

Several VDDT sensors are utilised, two of which are with a decent SRAM serving as a reference, and another with the SRAM that is being tested serving as a target for testing, and a third with an SRAM that is not being tested serving as a target for testing, respectively (see Figure 1). When the outputs from both sensors are compared, it is possible to tell which sensor works better. This is accomplished by using a comparator to determine which sensor performs superior. If an SRAM failure happens, as a consequence of the change in transient current as a result of the failure, the outputs of the operational amplifiers will be prone to fluctuation, which is not ideal in

ISSN:0975-3583,0976-2833 VOL10,ISSUE04,2019

this case. As a result of the process, a second pulse is formed at the comparator's output, resulting in an additional pulse being generated. Using the same circuitry to evaluate a single SRAM cell as well as an array of SRAM cells at the same time can save time and money compared to using a separate circuitry for each SRAM cell. In particular, when testing a large number of SRAM cells at the same time, this feature comes in handy.

IV. Simulation Results

A. Sensor Output

It is the task of pmos M1 to detect and record the transient current. Figure 5 depicts the voltage that has been detected by the use of the symbol V (voltage). (SENSE). Spikes emerge every 50ns in this case due to the fact that a write operation is executed once every 50ns in this example. Additionally, transient current flows during the entire writing procedure as an extra feature. The sensor's output is represented by the letter V on the graphical display. (OP). During write operations, a transitory current builds up, which is then converted to voltage after the process is complete.

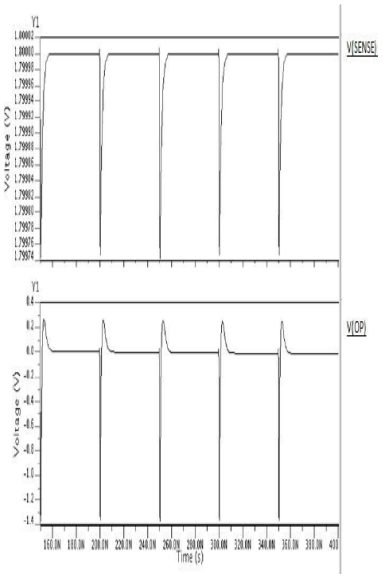


Figure 5 . Output of Vddt sensor implementation

Because of the presence of a defect in an SRAM, the transient current flowing during a transition writing process is altered. The difference in transient current between a defective and a fault-free SRAM is seen in Figure 6.

ISSN:0975-3583,0976-2833 VOL10,ISSUE04,2019

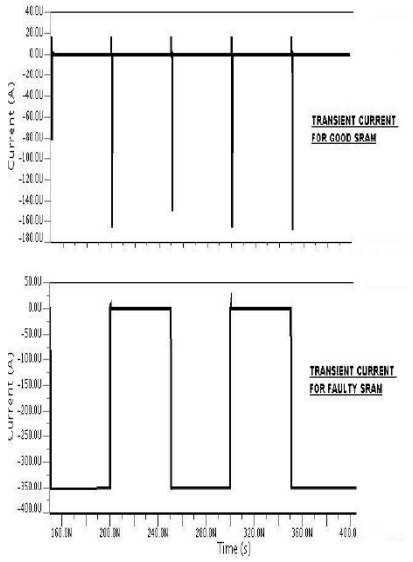
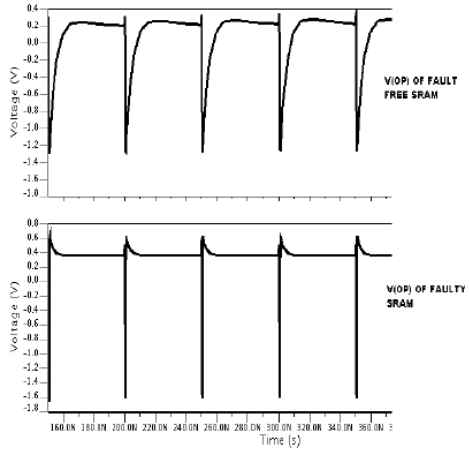


Figure 6 . Difference in transient current



Every SRAM, whether defective and fault-free, generates an oscillating output from the VDDT sensor in response to a transient current generated by the respective SRAM. Using the example of Figure 7, you can see how this variation works in action.

IV. CONCLUSIONS

This research presents an SRAM testing circuit that employs a transient current technique for fault detection. The efficacy of the circuit is assessed using a basic memory architecture with single and multiple faults, and the results show that the circuit is successful.

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